This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

Claims 7-15 and 24-31 are pending in the present application. Claims 7-9 and 24-27 have been amended. Claims 28-31 have been presented herewith.

Status of Current Office Action

On the Office Action Summary Form PTOL-326 received along with the current Office Action dated March 24, 2004, the Examiner indicated that prosecution as to the merits of the present application is closed in accordance with the practice under Ex parte Quayle. However, the claims have been rejected in the current Office Action in view of prior art. Also, on page 7 of the current Office Action, the Examiner indicated that a shortened statutory period of three (3) months has been set in which to respond to the current Office Action.

During a telephone conversation on April 19, 2004, Examiner Le acknowledged that the Office Action dated March 24, 2004, is **a Non-Final Office Action**, not a Quayle Action. The Examiner confirmed that a three (3) month shortened statutory period for response has been set.

Priority Under 35 U.S.C. 119

Enclosed is a copy of a Claim of Priority Letter dated April 20, 1998, filed in parent application Serial No. 09/062,720. Also enclosed is a dated, stamped postcard

receipt provided as evidence that the above noted Claim of Priority Letter was received by the U.S. Patent Office. **The Examiner is respectfully requested to acknowledge receipt of the priority document in parent application Serial No. 09/062,720, and to confirm on the record that the Claim for Priority in the present application is complete**.

Claim Rejections-35 U.S.C. 102(e)

Claims 7-15 and 24-27 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Miyazaki et al. reference (U.S. Patent No. 6,642,083). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method of manufacturing a semiconductor device of claim 7 includes in combination "preparing said semiconductor package..., wherein said connecting pattern is exposed at a peripheral area of said through hole", "electrically connecting the exposed portion of said connecting pattern and said electrode of said semiconductor element via wires through said through hole", and "sealing said through hole, the exposed portion of said connecting pattern and said wires with resin". Applicant respectfully submits that the Miyazaki et al. reference as relied upon by the Examiner does not disclose these features.

As described beginning in column 11, line 54 of the Miyazaki et al. reference with

respect to Fig. 2, flexible wiring substrate 3 includes tape 9 as the base material of the flexible wiring substrate, and wirings 10 bonded on the main surface of tape 9 by adhesive 9'. As further described, tape 9 is made of a material such as a polymide resin, whereby a material such as copper is used as the core material for wiring 10. A nickel plating layer may be used to cover the surface of the core material, and a gold plating layer may be additionally formed so as to cover the surface of the nickel plating layer.

As further described beginning in column 12, line 41 of the Miyazaki et al. reference, flexible wiring substrate 3 may be prepared as a TAB (tape automatic bonding) tape, by bonding a thin metal foil such as copper on tape 9 by means of an adhesive, forming a required pattern by photoresist on the metal foil using a photographic technique, and then forming a desired wiring pattern 10 by etching **(including also leads 11)**. A nickel-gold plating treatment may then be applied to a surface of the desired wiring pattern 10, and leads 11.

Accordingly, as may be readily understood in view of the above noted description, wirings 10 and leads 11 of the Miyazaki et al. reference are integral parts of the flexible wiring substrate 3. Leads 11 are merely formed by etching tape 9 away from flexible wiring substrate 3. Wiring 10 and lead 11 in the Miyazaki et al. reference are a continuous segment of copper. That is, wiring 10 and lead 11 are not separate elements or parts connected (bonded) together, but are merely a single contiguous

segment of copper.

In contrast, the method of manufacturing a semiconductor device of claim 7 includes in combination "electrically connecting the exposed portion of said connecting pattern and said electrode of said semiconductor element via wires through said through hole". That is, the connecting pattern and the wires in the method of manufacturing a semiconductor device of claim 7 are respectively different elements that are connected together. This is contrast to wiring 10 and lead 11 of the Miyazaki et al. reference which are a continuous segment.

As also described beginning on page 15, line 14 of the present application with respect to Fig. 4, connecting (wire bonding) is carried out between electrodes 38 within the through hall 35 in the substrate 33, and the corresponding end portions 34a of the connecting patterns 34 on the other side of substrate 33. That is, wires 39 are respectively connected to electrodes 38 and end portions 34a of connecting patterns 34, and wires 39 traverse through hall 35. As further described beginning on page 16, line 18 of the present application, since semiconductor element 32 and substrate 33 are bonded with wires, wires 39 can absorb the difference of the coefficient of thermal expansion between semiconductor element 32 and substrate 33, so that an inexpensive resin substrate may be used instead of an expensive ceramic substrate.

Accordingly, Applicant respectfully submits that the method of manufacturing a semiconductor device of claim 7 distinguishes over the Miyazaki et al. reference as

relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 7-15, is improper for at least these reasons.

The method of manufacturing a semiconductor device of claim 24 includes in combination "forming a plurality of connecting patterns on the second surface of said substrate, each of said connecting patterns having a first end that is exposed at a peripheral area of said elongate opening", "respectively electrically connecting said electrodes to corresponding ones of the first ends of said connecting patterns by plurality of wires extending from said elongate opening of said substrate to the peripheral area", and "covering said electrodes, said wires, and the first ends of said connecting patterns with a resin".

The method of manufacturing a semiconductor device of claim 26 includes in combination "forming a plurality of connecting patterns on the second surface of said substrate, each of said connecting patterns having a first end that is exposed at the bottom of said second elongate opening", "respectively electrically connecting said electrodes to corresponding ones of the first ends of said connecting patterns by plurality of wires extending from said first elongate opening to said second elongate opening of said substrate", and "covering said electrodes, said wires, and the first ends of said connecting patterns with a resin".

As emphasized above with respect to claim 7, wirings 10 and leads 11 of the Miyazaki et al. reference are integral parts of the flexible wiring substrate 3. Leads 11

are merely formed by etching tape 9 away from flexible wiring substrate 3. Wiring 10 and lead 11 in the Miyazaki et al. reference are a continuous segment of copper. That is, wiring 10 and lead 11 are not separate elements or parts connected (bonded) together, but are merely a single continuous segment of copper. The Miyazaki et al. reference as relied upon by the Examiner therefore does not disclose electrically connecting electrodes to connecting patterns by a plurality of wires, as respectively featured in claims 24 and 26. Applicant therefore respectfully submits that the method of manufacturing a semiconductor device of respective claims 24 and 26 distinguish over the Miyazaki et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 24-27, is improper for at least these reasons.

Claims 28-31

Applicant respectfully submits that claims 28-31, as respectively dependent upon claims 7, 24 and 26, distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, for at least the same respective reasons as set forth above and by further reason of the features therein.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the

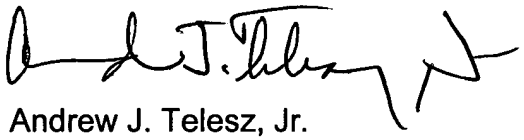
corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: Copy of Claim of Priority Letter
Copy of dated, stamped postcard receipt

OIPE JC25
JUN 16 2004
PATENT & TRADEMARK

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re Patent Application of

Takaaki SASAKI

Attn: Applications Branch

Serial No. [NEW]

Attorney Docket No. PNET.011

Filed: April 20, 1998

For: SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN, AND MANUFACTURING METHOD THEREOF

CLAIM OF PRIORITY

Honorable Assistant Commissioner for Patents and Trademarks,
Washington, D.C. 20231

Sir:

Applicant in the above-identified application, hereby claims the priority date under the International Convention of the following Japanese application:

Appln. No. 9-190818 filed July 16, 1997

as acknowledged in the Declaration of the subject application.

A certified copy of said application is being submitted herewith.

Respectfully submitted,

JONES & VOLENTINE, L.L.P.

Adam C. Volentine
Registration No. 33,289

JONES & VOLENTINE, L.L.P.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Tel. (703) 715-0870

Dated: April 20, 1998

OIPE JC25
JUN 16 2004
PATENT & TRADEMARK OFFICE

日 本 国 特 許 庁
PATENT OFFICE
JAPANESE GOVERNMENT

別紙添付の書類に記載されている事項は下記の出願書類に記載されてる事項と同一であることを証明する。
This is to certify that the annexed is a true copy of the following application as filed this Office.

願年月日 e of Application:	１９９７年　７月１６日
願番号 lication Number:	平成　９年特許願第１９０８１８号
願人 cant (s):	沖電気工業株式会社

１９９７年１２月　５日

特許庁長官
Commissioner,
Patent Office

荒井寿光

OIPE JUN 16 2004 PATENT & TRADEMARK OFFICE

APR 20 1998 PAT. & TRADEMARK OFF.

REQUEST FOR EARLY NOTIFICATION OF SERIAL NUMBER

ATTY DOCKET #: PNET.011 **DUE DATE:** July 16, 1998

APPLICANT: Takaaki SASAKI

SERIAL NO.: (NEW) **FILING DATE:** April 20, 1998

TITLE: SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN, AND MANUFACTURING METHOD THEREOF

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED:

New U.S. Patent Application including: Patent Application Transmittal Form with $830 filing fee; Recordation Form Cover Sheet with executed Assignment (3 pages); specification, claims and abstract (30 pages); executed Declaration and Power of Attorney (3 pages); drawings (6 sheets; FIGS. 1-9); and Claim of Priority including 1 Japanese application; Preliminary Amendment.

DATE: April 20, 1998 **ATTY:** ACV **[Check No. 5443]**